A2 amended

7. Receiver arrangement according to claim 1, characterized in that the demodulator circuit arrangement (18) has as the output stage an offset stage (21), which is connected to a voltage signal output of a demodulator circuit (20) of the demodulator circuit arrangement (18) in order to adapt the output signal of the demodulator circuit arrangement (18) to the input stage (22) of the signal-processing circuit arrangement (23).

A3

9. Receiver arrangement according to Claim 7, characterized in that the offset stage (21) is set by the control circuit arrangement (12) during setting operation on the basis of its output signal.

10. Receiver arrangement according to Claim 7, characterized in that the control circuit arrangement (12) is assigned a memory (31) in which a value for a direct voltage offset to be set, determined during the setting operation on the basis of the output signal of the offset stage (21), is stored, and in that the offset stage (21) can be set by the control circuit arrangement (12) to correspond to the stored value.

REMARKS

In accordance with 37 C.F.R. §1.121 (as amended on 11/7/2000) the rewritten claim(s) above are shown on separate page(s) marked up to show all the changes relative to the previous version of that section.

Respectfully submitted,

10 April 01

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Date

Application entitled: RECEIVER ARRANGEMENT FOR RECEIVING FREQUENCY-MODULATED RADIO SIGNALS AND METHODS OF ADAPTING AND TESTING A RECEIVING BRANCH OF THE RECEIVER ARRANGEMENT

MARKED UP CLAIM(S)

3. Receiver arrangement according to Claim 1 ~~or 2~~, characterized in that the test-signal generator stage (28) comprises a frequency divider (30), which supplies as the output signal a frequency signal which contains a harmonic with a first frequency equal or virtually equal to the intermediate frequency.

5. Receiver arrangement according to Claim 3 ~~or 4~~, characterized in that the clock signal output of the clock-signal oscillator (26) is applied to the frequency dividers (30, 32) via in each case one of the switches (29, 33) which can be controlled by the control circuit arrangement.

6. Receiver arrangement according to ~~one of the preceding claims~~claim 1, characterized in that the demodulator circuit arrangement (18) has as the input stage a bandpass filter (19), and in that the fundamental frequency of the test signal is greater than the bandwidth of the bandpass filter (19), preferably greater than twice the bandwidth, in particular greater than four times the bandwidth of the bandpass filter (19).

7. Receiver arrangement according to ~~one of the preceding claims~~claim 1, characterized in that the demodulator circuit arrangement (18) has as the output stage an offset stage (21), which is connected to a voltage signal output of a demodulator circuit (20) of the demodulator circuit arrangement (18) in order to adapt the output signal of the demodulator circuit arrangement (18) to the input stage (22) of the signal-processing circuit arrangement (23).

9. Receiver arrangement according to Claim 7 ~~or 8~~, characterized in that the offset stage (21) is set by the control circuit arrangement (12) during setting operation on the basis of its output signal.

10. Receiver arrangement according to Claim 7 ~~or 8~~, characterized in that the control circuit arrangement (12) is assigned a memory (31) in which a value for a direct voltage offset to be set, determined during the setting operation on the basis of the output signal of the offset stage (21), is stored, and in that the offset stage (21) can be set by the control circuit arrangement (12) to correspond to the stored value.